孕龍科技股份有限公司
Zeroplus Technology Co., Ltd.

SPECIFICATION

MODEL: B08009-LAP-SLE4442-M

PART NO： _____

VERSION： V1.22

Approver		Check	Design
GM	PM		

Customer Confirm

＊Please fax the file to Zeroplus Technology after signing.

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Content

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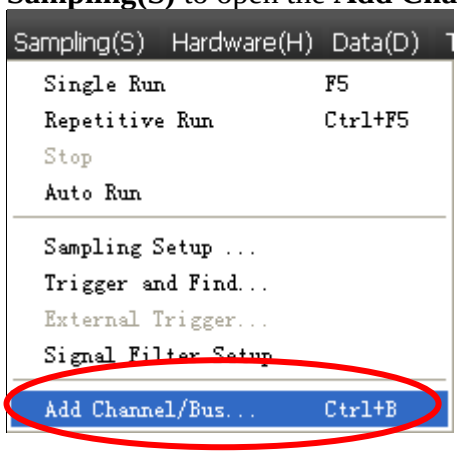
1 Software Register

Please register the software as the following steps:

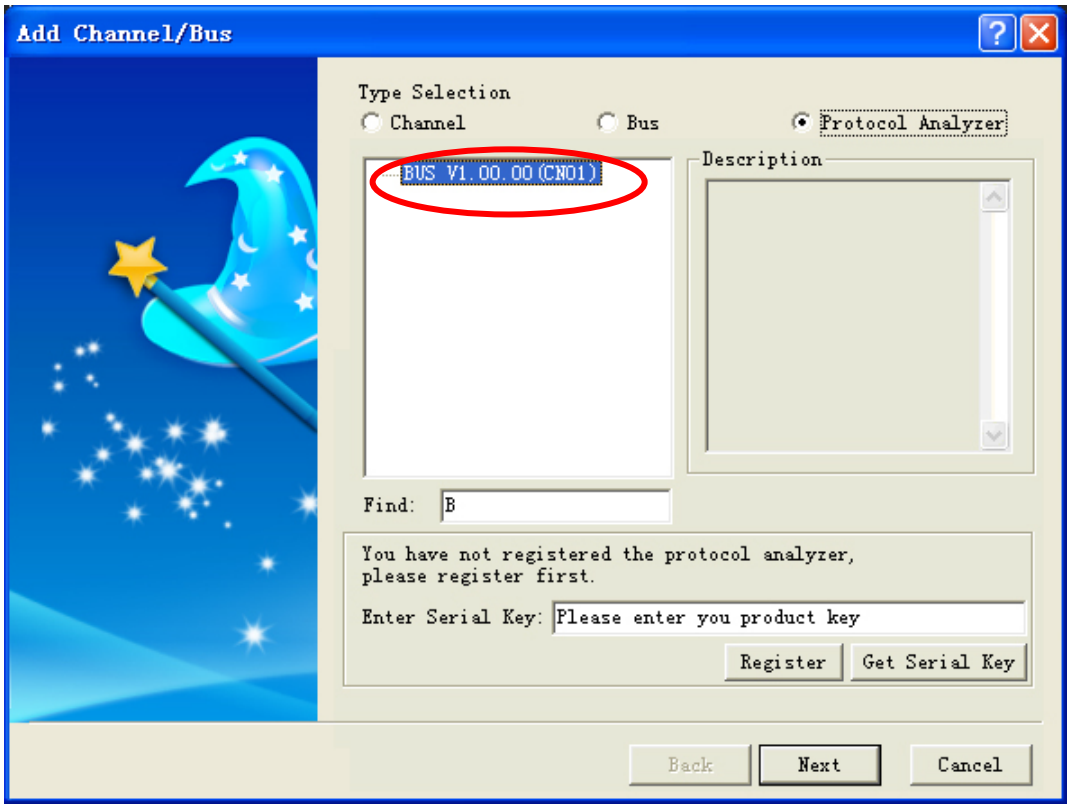
※ Remark1: The registration steps for all protocol analyzers are the same; you can complete the registration by following procedures. Following is an example on how to register the Protocol Analyzer BUS.

※ Remark2: We won't have additional notice for you, when there is any modification of the module specification. If there is some unconformity caused by the module version upgrade, users should take the module software as the standard.

STEP 1. Open the Logic Analyzer and select the **Add Channel/Bus** item on the pull-down menu of the **Sampling(S)** to open the **Add Channel/Bus** dialog box.



STEP 2. Select Protocol Analyzer item in the Add Channel/Bus dialog box, expand the Other Type, and select the BUS.



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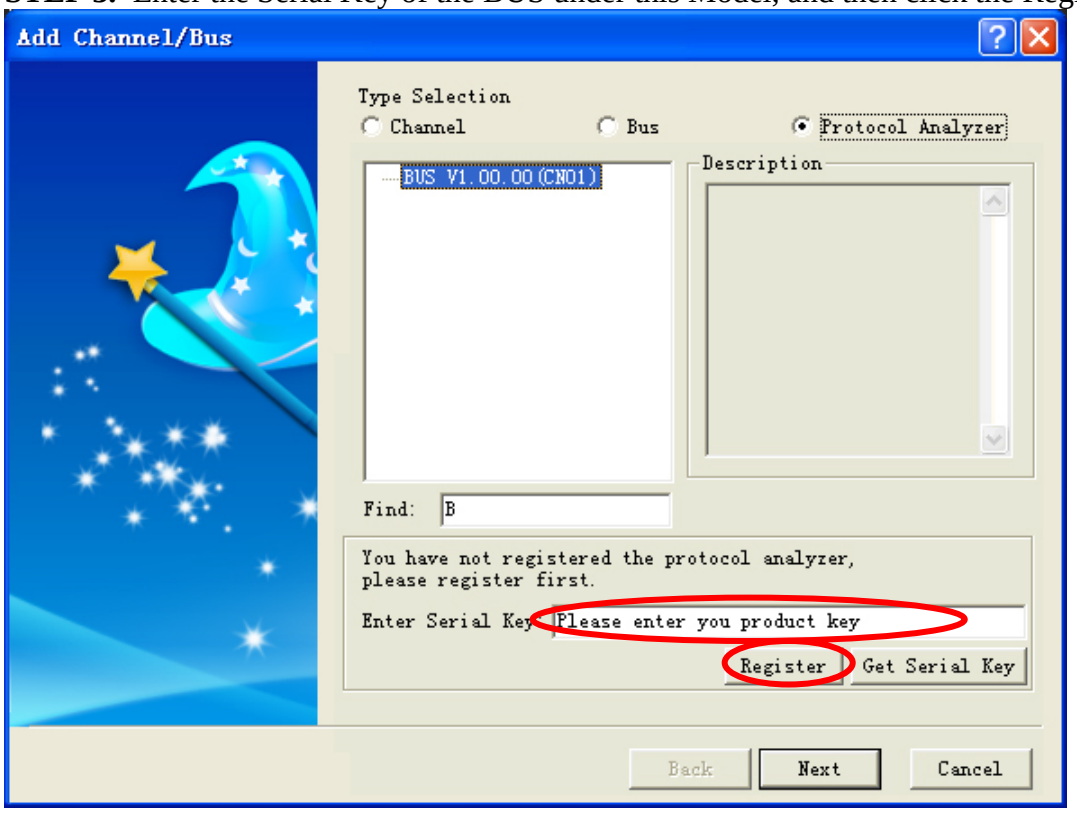
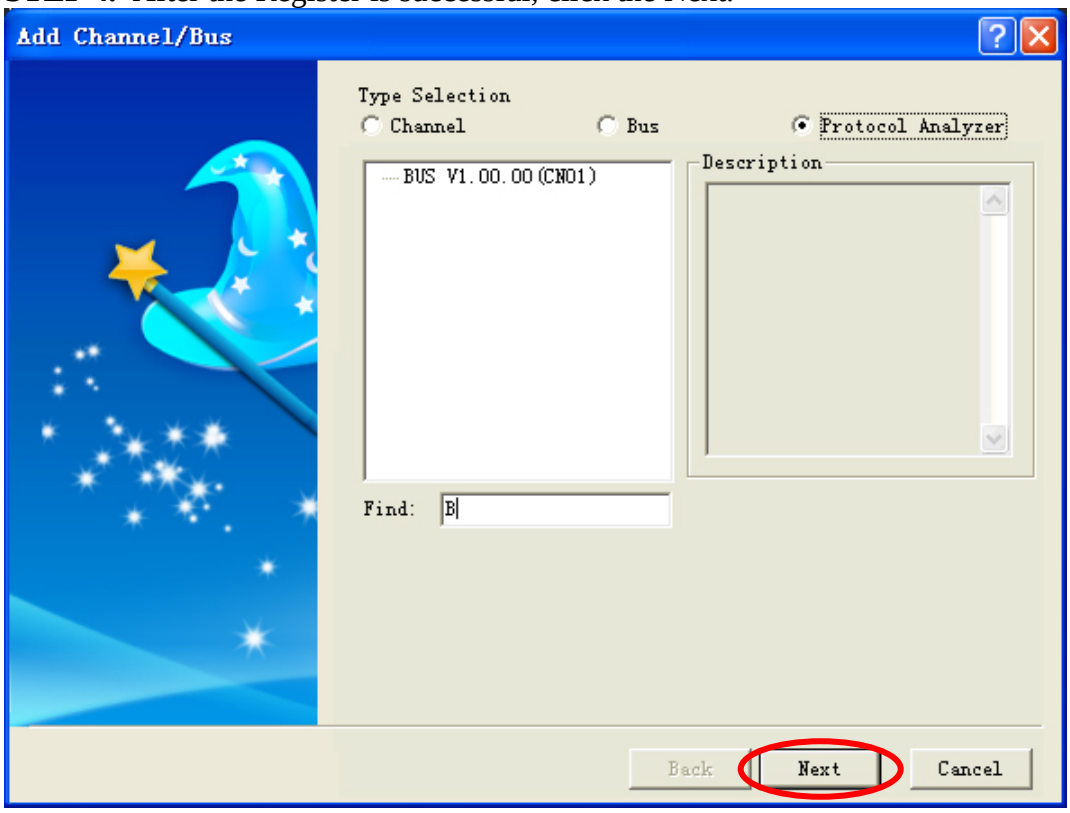
STEP 3. Enter the Serial Key of the BUS under this Model, and then click the Register.



STEP 4. After the Register is successful, click the Next.



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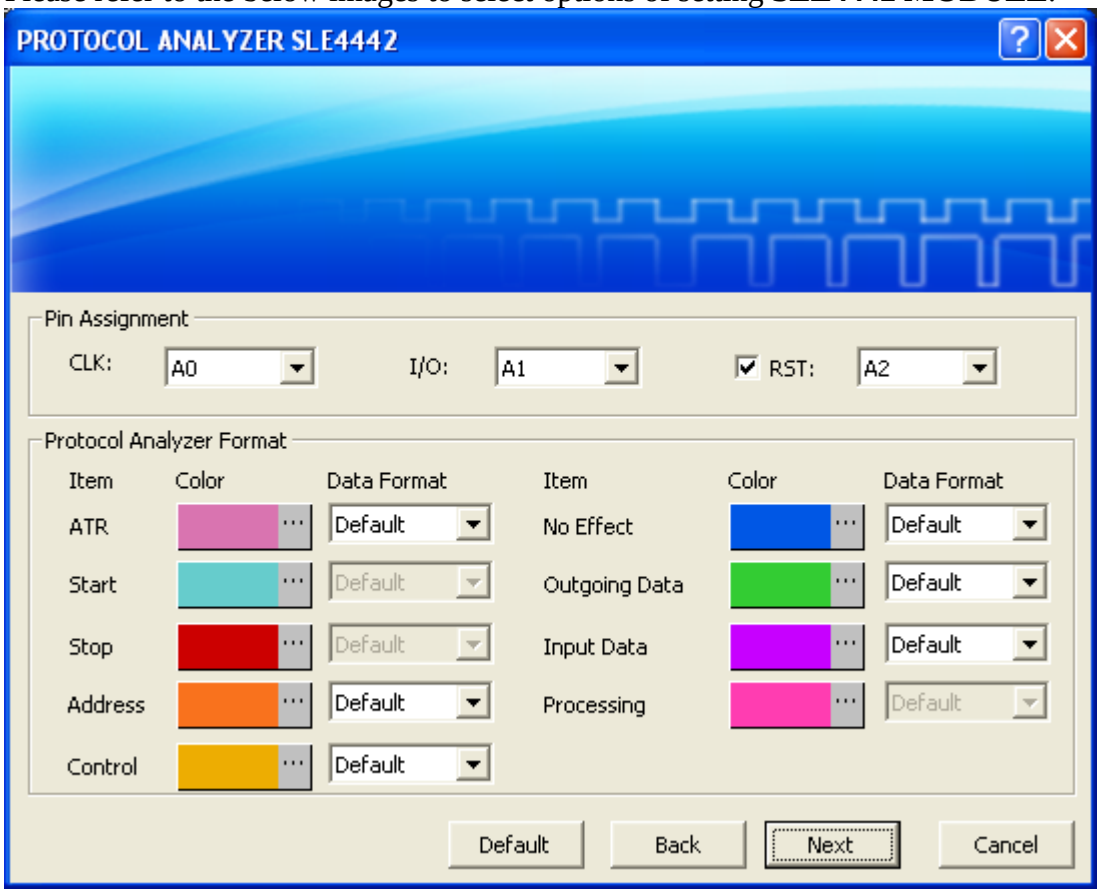
2 User Interface

Please refer to the below images to select options of setting **SLE4442 MODULE**.



Pin Assignment:
Selection of Protocol Analyzer SLE4442 channels:
1. CLK is the clock signal line, and its default is A0.
2. I/O is the data signal line, and its default is A1.
3. RST is the reset signal line, and its default is A2.

When the RST is selected, the decoding is the 3-line mode, and the value of I/O is read as the CLK is Rising Edge. When the RST is not selected, the decoding is 2-line mode, and the default of RST is Low; the value of I/O is also read as the CLK is Rising Edge.

Protocol Analyzer Format:
The color of the protocol analyzer can be varied by users. Users can set the Data Format of the ATR, Address, Outgoing Data, Control, Input Data, No Effect as their requirements. When selecting the option, Activate, the data format is decided by the settings in the Protocol Analyzer; when not selecting the option, Activate, the data format is decided by the settings in the main program.

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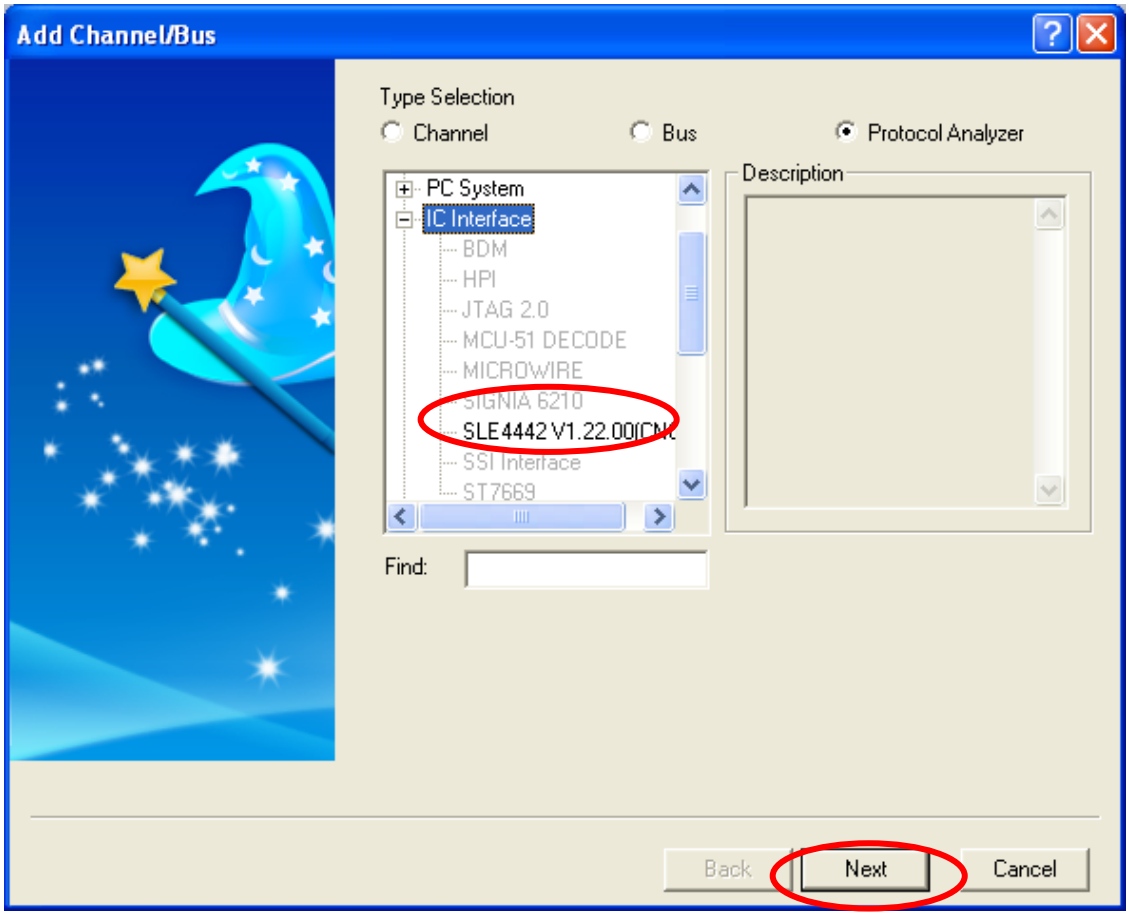
3 Operating Instructions

STEP 1: Select the Add Channel/Bus item on the pull-down menu of the Sampling(S) to open the Add Channel/Bus dialog box.

STEP 2: Select the Protocol Analyzer item in the Add Channel/Bus dialog box, expand the IC Interface, select the SLE4442 and then click Next.



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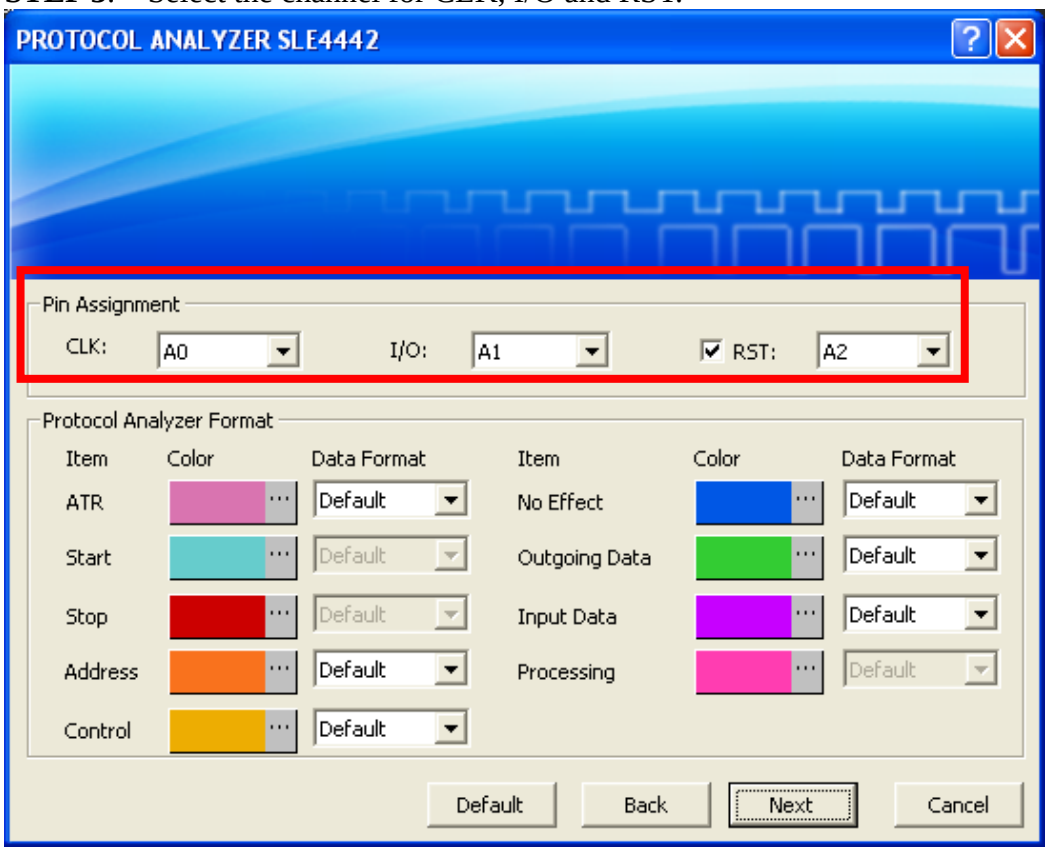
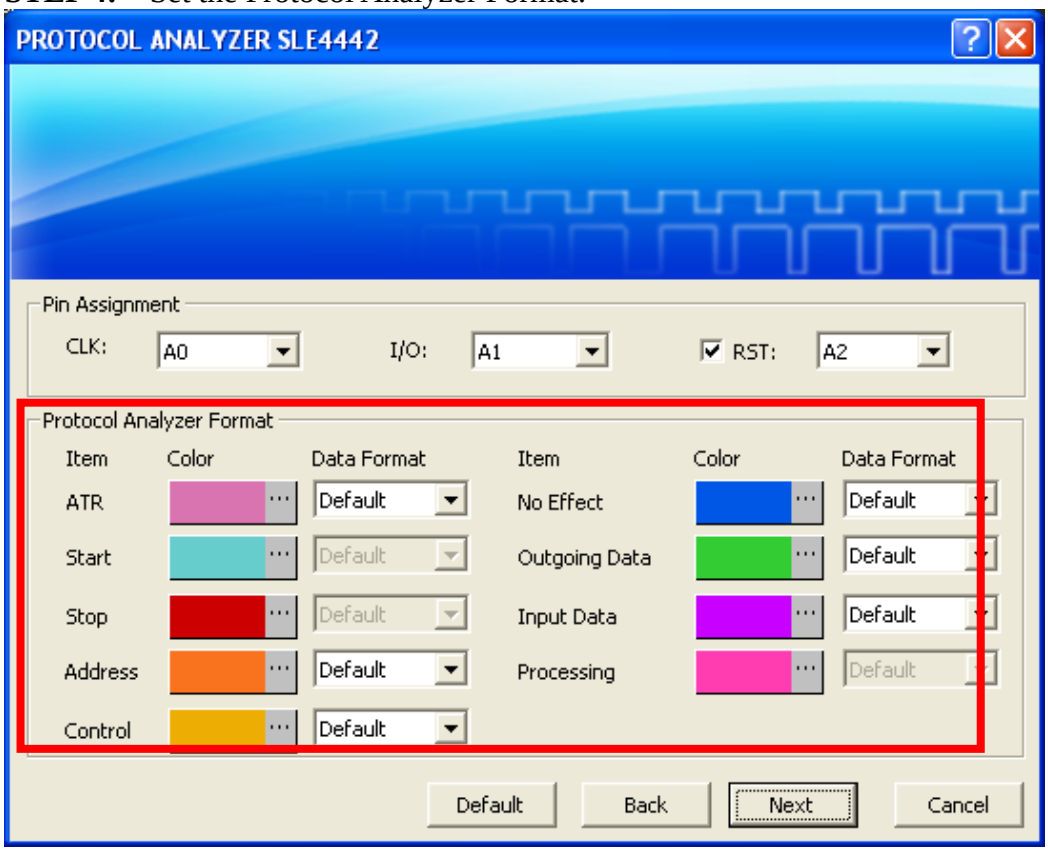
STEP 3: Select the channel for CLK, I/O and RST.



STEP 4: Set the Protocol Analyzer Format.



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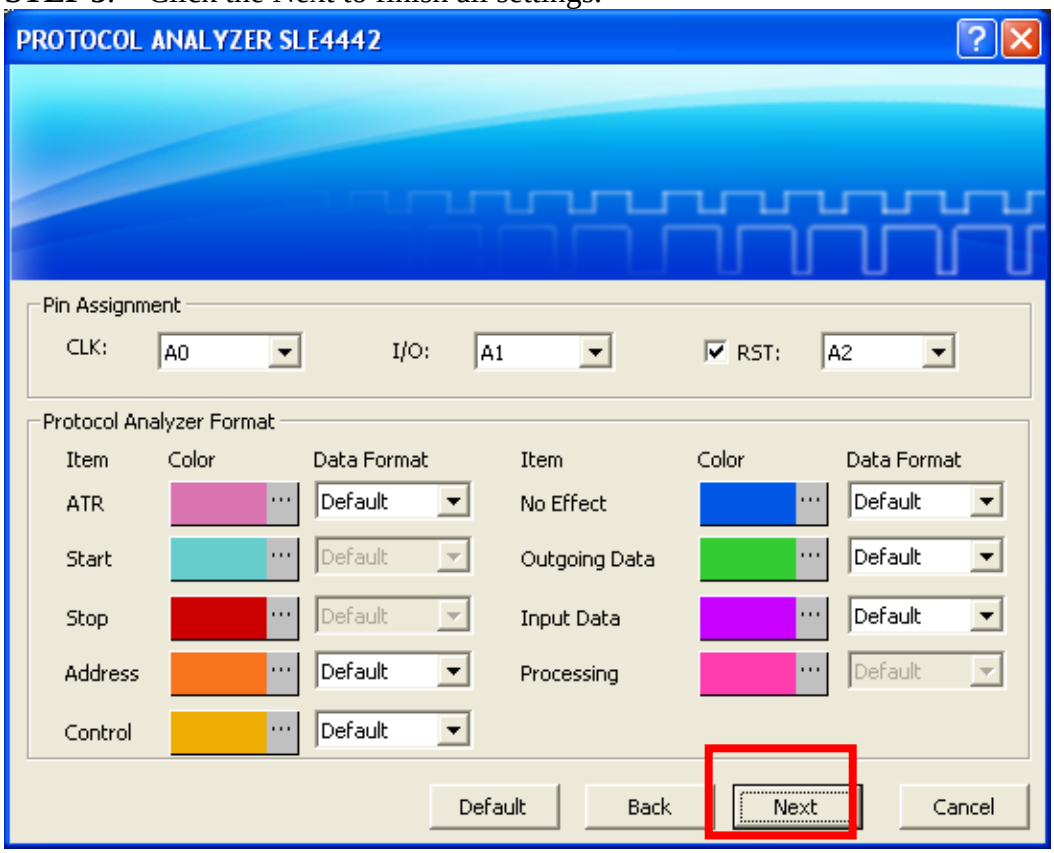
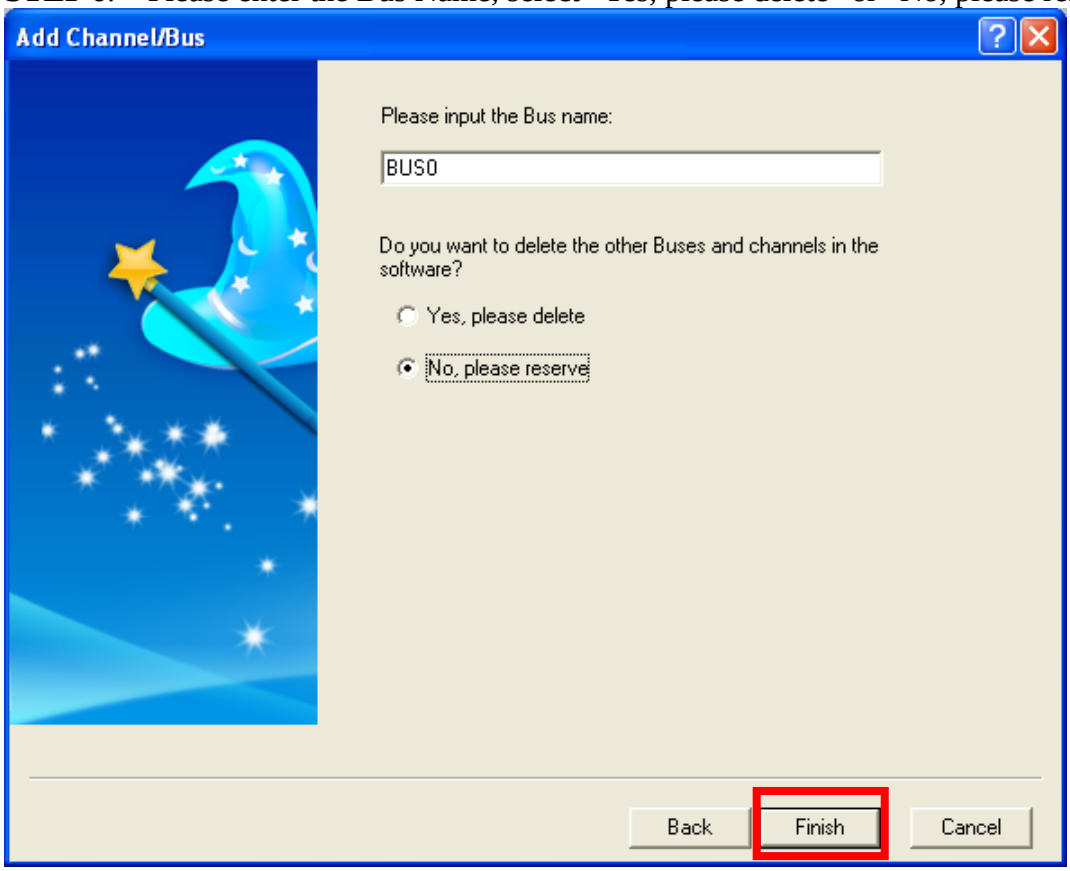
STEP 5: Click the Next to finish all settings.



STEP 6: Please enter the Bus Name, select “Yes, please delete” or “No, please reserve” and then click Finish.



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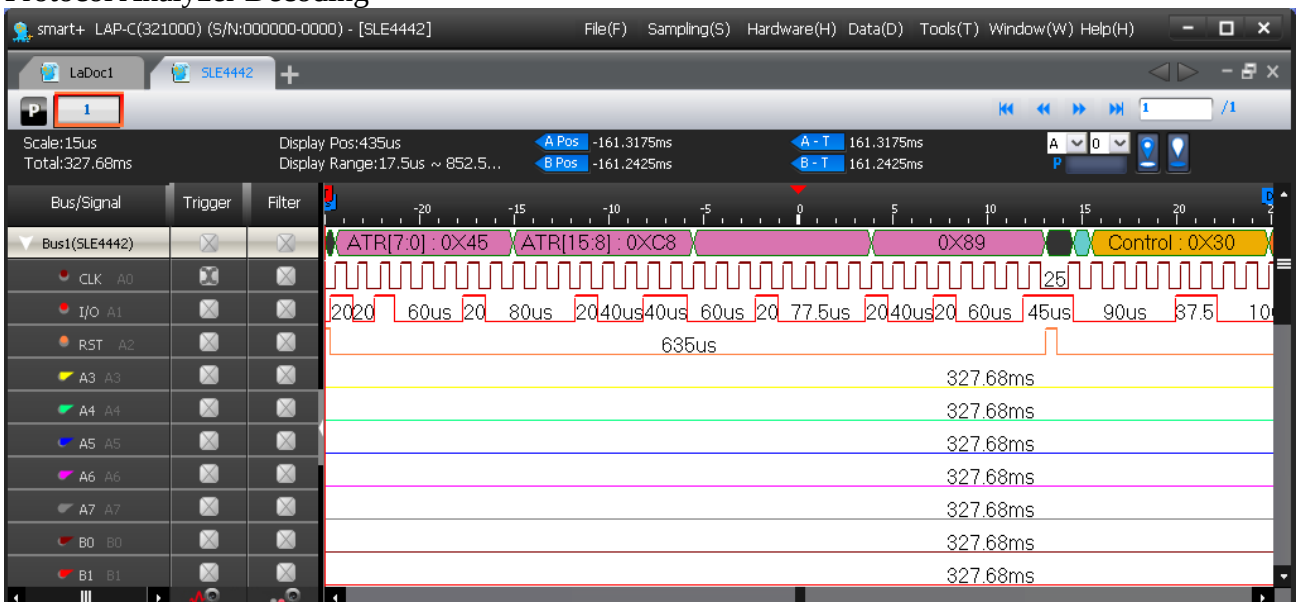
STEP 7: Following pictures show the completion of the protocol analyzer decoding and the packet list. The trigger condition is set as Either Edge; the memory depth is 128K; the sampling frequency is 400KHz (the sampling frequency should be more than eight times higher than the signal to be tested).

Protocol Analyzer Decoding



Packet List